Version with Markings to Show Changes Made

In the Specification:

The paragraph beginning at page 3, line 3 has been amended as follows:

> Applicants have discovered that by carefully controlling the arrangement spacing and layering of certain signal traces in an LVD SCSI bus that noise problems [effecting] affecting bus performance may be significantly reduced. Techniques which may be employed individually or collectively include running RESET, SELECT and BUSY signal trace pairs in adjacent relationship; providing increased separation of RESET, SELECT and BUSY signal trace pairs from the other bus signal traces; running at least a portion of RESET, SELECT and/or BUSY signal trace pairs on a side of the associated PCSB opposite from the side where other bus signal traces are run.

The paragraph beginning on page 7, line 8 has been amended as follows:

> The PCSB 10 comprises a board 12, Figs. 1 and 2, made up of multiple component layers which may each have electrical circuitry provided therein. The circuitry may be interconnected between layers by conductors, known as vias, which extend perpendicularly through the board. A typical PCSB in a personal computer may have 4 to 6 component layers. A typical PCSB in a computer work station

or server may have 8 to 10 or more layers. Printed circuit [boards] board construction, as generally described immediately above, is well known in the art. The [Board] board 12 shown in the drawings comprises a first surface layer or "top" layer 14, a second surface layer or "bottom" layer 16 and a plurality of intermediate layers positioned between layers 14 and 16. (It is to be understood that the terms "top" and "bottom" are used herein because they are familiar reference terms which facilitate description of the preferred embodiments of the invention. However these terms are entirely arbitrary and are not to be construed in a manner which in any way limits the scope of the invention.) One of the intermediate layers may comprise a ground plane (not shown) constructed from a thin layer of copper or the like. The board has a peripheral portion 22 and a central portion 24. The peripheral portion 22 terminates at a plurality of interconnected, linear, peripheral edge portions 26, 28, 30, 32, 34, 36, 38, 40, 42, 44.

The paragraph beginning on page 7, line 8 has been amended as follows:

The second plurality of signal traces 144 may follow the same trace path 141 as the first plurality of signal traces 142. The difference, however, is that the second plurality of traces 144 extend along at least a portion of this path in the surface layer 14 opposite to the surface layer 16 in which the entire length of the first plurality of signal traces 142 is contained. This second set of

signal traces 144 comprises fewer signal pairs than the first plurality of signal traces 142 and preferably includes at least the RESET signal pair 170, the SELECT signal pair 172, and the BUSY signal pair 174. The RESET, SELECT, and BUSY signal pair traces are preferably positioned next adjacent one another the entire length of the signal bus[.], i.e., no other bus signal traces are positioned between any two of the RESET, SELECT, and BUSY signal pairs.

In the claims:

Claim 1 has been amended as follows:

1. (once amended) A PCSB assembly comprising:

a PCSB;

a first plurality of LVD SCSI bus signal trace pairs formed in said PCSB; and

a second plurality of LVD SCSI bus signal trace pairs formed in said PCSB [and positioned next adjacent one another for the entire length thereof] comprising a RESET signal trace pair, a SELECT signal trace pair and a BUSY signal trace pair and wherein said RESET signal trace pair, said SELECT signal trace pair and said BUSY signal trace pair are positioned next adjacent one another for the entire length thereof.

Claim 5 has been amended as follows:

5. (once amended) The PCSB assembly of claim 1

wherein said PCSB comprises a first exterior surface layer and a second exterior surface layer opposite said first exterior surface layer and wherein said first plurality of LVD SCSI bus signal trace pairs are positioned in said first exterior surface layer and wherein said second plurality of LVD SCSI bus signal trace pairs are positioned at least partially in said second exterior surface layer [pair].

Claim 8 has been amended as follows:

8. (once amended) The PCSB assembly of claim 2 wherein said PCSB comprises a first exterior surface layer and a second exterior surface layer opposite said first exterior surface layer and wherein said first plurality of LVD SCSI bus signal trace pairs are positioned in said first exterior surface layer and wherein said second plurality of LVD SCSI bus signal trace pairs are positioned at least partially in said second exterior surface [pair] layer.

Claim 11 has been amended as follows:

11. (once amended) A PCSB comprising[;]:

a first surface layer comprising a plurality of LVD SCSI bus signal trace pairs; and

a second surface layer opposite said first surface layer comprising at least a portion of at least one signal trace pair selected from the group of: a LVD SCSI bus RESET signal trace pair; a LVD SCSI bus SELECT signal trace pair and a LVD SCSI bus BUSY signal trace pair; and excluding all LVD SCSI bus signal trace pairs other than

those in said group.